IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

Ocean Semiconductor LLC, Plaintiff v. MediaTek Inc. and MediaTek USA Inc. ("MediaTek"), Defendants.	Civil Action No.: 6:20-cv-1210-ADA JURY TRIAL DEMANDED PATENT CASE
Ocean Semiconductor LLC, Plaintiff v. NVIDIA Corporation, Defendant.	Civil Action No.: 6:20-cv-01211-ADA JURY TRIAL DEMANDED PATENT CASE
Ocean Semiconductor LLC, Plaintiff v. NXP USA, Inc. Defendant.	Civil Action No.: 6:20-cv-1212-ADA JURY TRIAL DEMANDED PATENT CASE

Ocean Semiconductor LLC, Plaintiff v. Renesas Electronics Corporation and Renesas Electronics America, Inc., Defendants.	Civil Action No.: 6:20-cv-1213-ADA JURY TRIAL DEMANDED PATENT CASE
Ocean Semiconductor LLC, Plaintiff v. Silicon Laboratories Inc., Defendant.	Civil Action No.: 6:20-cv-1214-ADA JURY TRIAL DEMANDED PATENT CASE
Ocean Semiconductor LLC, Plaintiff v. STMicroelectronics, Inc., Defendant.	Civil Action No.: 6:20-cv-1215-ADA JURY TRIAL DEMANDED PATENT CASE

Ocean Semiconductor LLC, Plaintiff v. Western Digital Technologies, Inc. Defendant.	Civil Action No.: 6:20-cv-1216-ADA JURY TRIAL DEMANDED PATENT CASE

DECLARATION OF RON MALTIEL IN SUPPORT OF PLAINTIFF OCEAN SEMICONDUCTOR LLC'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

I. INTRODUCTION

1. My name is Ron Maltiel and I have been retained by Plaintiff Ocean Semiconductor LLC ("Ocean" or "Plaintiff") as an expert witness in litigations against MediaTek Inc. and MediaTek USA Inc, NVIDIA Corporation, NXP USA, Inc., Renesas Electronics Corporation and Renesas Electronics America, Inc., Silicon Laboratories Inc., STMicroelectronics, Inc., and Western Digital Technologies, Inc. (collectively, "Defendants")

2. I have been asked to render opinions on claim terms and/or phrases that have been identified for claim construction by Defendants and Plaintiff of the following patents that I understand are each at issue in one or more of the litigations: U.S. Patents No. 6,420,097 ("'097 patent"), 6,660,651 (the "'651 patent"), and 8,676,538 (the "'538 patent") (together, "the Asserted Patents").

3. This report contains statements of my opinions formed to date regarding these patents and the bases and reasons for those opinions. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses.

4. I reserve the right to revise, supplement, and/or amend my opinions in this declaration based on future positions taken by Defendants and/or their experts, additional documents, testimony, or other information provided by Defendants or its witnesses, any orders from the Court, or as I may otherwise find necessary and to offer rebuttal analyses and/or opinions to any such positions of the Defendants.

5. My educational and professional background, patents, and professional association memberships are listed in my curriculum vitae, which is attached as Exhibit 1 to this declaration.

II. QUALIFICATIONS

6. Based on the following qualifications and experience, I believe I am qualified to offer opinions how one of ordinary skill in the art at the relevant time would construe various terms included in any of the Asserted Patents.

7. I am a senior member of the Institute of Electrical and Electronics Engineers (IEEE) with more than 30 years of experience in all phases of design and implementation of computer semiconductor devices. I have worked in the development and production of semiconductor devices as well as storage technologies. My work has focused on the development, integration, and optimization of new processes and circuits into one final work product and introducing it to production.

8. I received a Bachelor of Science degree in Material Science and Engineering from Ben-Gurion University in 1977. I then went on to receive my Master of Science degree in Material Science and Engineering from Stanford University in 1978 and my Engineering Degree in Material Science and Engineering from Stanford in 1980. At Stanford University, an Engineer Degree is an additional graduate degree that can be earned following a Master's Degree. The degree differs from a Ph.D. in that an Engineer Degree's focus is primarily on professional engineering work as opposed to a Ph.D.'s primary focus on theoretical research or university teaching. An Engineer Degree requires two years of additional study beyond a Master's Degree and the completion of a thesis. My thesis related to semiconductor devices and electrical measurements of their properties.

9. Between 1978 and 1980, I was part of the Electrical Engineering research group on metallic impurities and their electrical behaviors. During this time I also conducted independent research on the manufacturing of Silicon devices and electrical measurements of their properties.

10. I worked for Intel Corporation from 1980 through 1982 on reliability and process integration of non-volatile memories. During that time I participated in the development of the first commercially available electronic erasable programmable read only memory, which is more commonly referred to as EEPROM. EEPROM technology was a non-volatile semiconductor memory that could be erased and programmed electrically. Its development came out of the standard EPROM technology that was widespread in the late 1970s and 1980s. EPROM semiconductor memories could not be erased electrically, but rather erasure was done by ultraviolet (UV) light. Thus EEPROM technology was a breakthrough commercial memory technology. EEPROM became a key foundation block for the development of flash memories a few years later.

11. After leaving Intel in 1982, I worked for American Microsystems, Inc. from 1982 through 1983 on the development of new process integration for EEPROM memories. During my employment at American Microsystems, I introduced and established their EEPROM device. I directed the design and testing of the EEPROM device. I further developed a new process to improve poly dielectric strength and founded a new memory cell structure with multiple benefits over the existing cells at that time.

12. I next worked for Advanced Micro Devices (AMD) in several areas between 1983 and 1989. While at AMD, I managed test chip development and helped develop a company-wide standard test chip library. This significantly reduced the time needed to build test chips at AMD. I further contributed to the development of 256K SRAM including the process flow and backend planarization scheme. I participated in defining the 1M CMOS DRAM memory and proved the feasibility of integrating trenches into the process. I further coordinated the development of post grove planarization process and double ploy module. I also developed the integration of

EEPROM with DRAM CMOS processes and devices. During this time I also helped reduce cell size by 40%, process steps by 15%, and improved programming operations.

13. After leaving AMD, I worked for Maxim Integrated Products developing all their CMOS processes between 1989 and 1993. During this time I personally developed a high voltage BICMOS device, introduced the device into production, and proved the feasibility of adding EEPROM to the BICMOS. While working for Maxim, I developed the company's newest analog process and installed the production in a new foundry.

14. I left Maxim in 1993 to start the semiconductor consulting company RMG and Associates. I have successfully managed RMG and Associates from 1993 through the present-day. At RMG and Associates, I have provided consulting across several aspects of semiconductor technology and manufacturing. I also operate a semiconductor website www.maltiel-consulting.com and a blog (with about 1200 readers) for more than 10 years which includes current developments in the digital and analog fields such as DRAM, Flash (NAND, NOR), SSD, EEPROM, ROM, and SRAM. On the website, I provide tutorials, educational information, industry news and resources, technical definitions, and patent search and application information. This website is regularly visited by major technology companies and universities from approximately 100 countries across the world.

15. I am the named inventor of six patents. The patents are in the areas of semiconductor manufacture. Three of my patents, for example, are related to creating new semiconductor devices. Two other patents are related to measurements of wafers during fabrication. The last patent is related to integrating resistors into doped regions in the semiconductor substrate. My patents have been referenced in other United States patents more than 130 times.

a. Electrical measurements of profile of semiconductor devices during their manufacturing process. U.S. Patent No. 4,978,923

b. Electrical measurements of properties of semiconductor devices during their manufacturing process. U.S. Patent No. 4,956,611

c. Memory cell providing simultaneous non-destructive access to volatile and non-volatile data. U.S. Patent No. 4,672,580

d. Non-volatile dynamic ram cell. U.S. Patent No. 4,611,309

e. Gold-doped IC resistor region. U.S. Patent No. 4,432,008

16. There are also many articles on my blog, listed above, in the technology areas of my expertise. Based upon my education, training and experience, as summarized above and set forth in my CV attached hereto as Exhibit 1, I believe I am qualified to provide opinion testimony as an expert on how the terms of the Asserted Patents proposed for construction would have been understood by person of ordinary skill in the relevant art ("POSITA") and that the identified terms are not indefinite (i.e., not insolubly ambiguous) .

17. In the past 5 years, I have testified as an expert witness in either deposition or trial in approximately 3 patent-related proceedings. I am available to appear live for testimony in support of my opinions. The opinions to which I will testify are based on the education, experience, training and skill that I have accumulated in the course of my career, as well as materials I have reviewed in connection with this matter.

III. PRIOR TESTIMONY

18. I have been retained as a testifying expert and technical consultant in connection with a number of patent litigation matters, including matters before U.S. District Courts and the United States Patent and Trademark Office Patent Trial and Appeal Board (PTAB).

19. A list of all such cases in which, during the previous 5 years, I have testified as an expert at trial or by deposition can be found in my CV (Exhibit 1).

20. In addition, I have previously offered opinions regarding the '538 patent as well as U.S. Patent Nos 6,907,305 (the "'305 patent") and 6,968,248 (the "'248 patent") (collectively, the "'305 and '248 patents"), 6,725,402 (the "'402 patent"), and 6,836,691 (the "'691 patent") in support of Ocean's briefs in opposition to Motions to Dismiss in *Ocean Semiconductor LLC V. Analog Devices, Inc.*, C.A. No. 1:20-cv-12310-PBS (D. Mass.), *Ocean Semiconductor LLC V. Infineon Technologies AG*, C.A. No. 1:20-cv-12311-PBS (D. Mass.), and in the above-captioned case against Renesas Electronics Corporation and Renesas Electronics America, Inc.

IV. COMPENSATION

21. I am being compensated for my services at a rate of $520 per hour. I am also being separately reimbursed for any out-of-pocket expenses. My compensation is not contingent upon the outcome of this matter or any opinions that I express herein. I have no other interests in these actions or with any party.

V. MATERIALS CONSIDERED

22. My opinions are based on my experience in this field, and are necessarily formed by my own experiences, materials I have read over the years, and discussions I have had with colleagues during my career. In addition, I have reviewed and considered the following materials in forming my opinion:

a. The '097 patent and its prosecution history;

b. The '651 patent and its prosecution history;

c. The '538 patent and its prosecution history;

d. Defendants' Opening Claim Construction Brief ("Defs.' Br."), and exhibits thereto;

e. Declaration of Costas Spanos, Ph.D. ("Spanos Dec.").

VI. LEGAL STANDARD

A. Person of Ordinary Skill in the Art (POSITA)

23. I understand that the hypothetical person of ordinary skill in the art ("POSITA") is considered to have the normal skills and knowledge of a person in a certain technical field, as of the time of the invention at issue. I understand that factors that may be considered in determining the level of ordinary skill in the art include: (1) the education level of the inventor; (2) the types of problems encountered in the art; (3) the prior art solutions to those problems; (4) rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the education level of active workers in the field. I also understand that "the person of ordinary skill" is a hypothetical person who is presumed to be aware of the universe of available prior art.

24. Based on these factors, it is my opinion that a POSITA for the '097 patent as of around 2000 is a person with (i) a B.S. in Engineering, Materials Science or a closely related field with three or more years of experience in semiconductor manufacturing or (ii) at least an M.S. in Engineering or Materials Science. Additional education or experience may serve as a substitute for these requirements.

25. Based on these factors, it is my opinion that a POSITA for the '651 patent as of around 2001 is a person with (i) a B.S. in Engineering, Materials Science or a closely related field with three or more years of experience in semiconductor manufacturing or (ii) at least an M.S. in Engineering or Materials Science. Additional education or experience may serve as a substitute for these requirements.

26. Based on these factors, it is my opinion that a POSITA for the '538 patent as of around 2004 is a person with (i) a B.S. in Engineering, Materials Science or a closely related field with three or more years of experience in either semiconductor manufacturing or advanced

process control or (ii) at least an M.S. in Engineering or Materials Science. Additional education or experience may serve as a substitute for these requirements.

27. The opinions I express herein are given from the point of view of a POSITA, as described above, at the time of the invention or claimed priority date of the each of the Asserted Patents. Even if I do not repeat this explicitly, this is the perspective that I applied in my analysis and in this declaration, unless I indicate otherwise.

B. Claim Construction

28. I have been informed that claim terms are presumed to have their ordinary and customary meaning. I understand the ordinary and customary meaning of a claim term to be the meaning understood by a person of ordinary skill in the art when read in the context of the patent's specification and prosecution history.

29. I have further been informed that a claim may be given a meaning that differs from the ordinary and customary meaning when: 1) the patentee sets out a definition and acts as his own lexicographer, or 2) the patentee disavows the full scope of the claim either in the specification or in prosecution.

30. I have also been informed that the intrinsic record of the patent may be used to interpret the meaning of a claim term. I understand that the intrinsic record of the patent includes both the patent's specification and its prosecution history. I understand that limitations should not be imported into the claims from the specification or the prosecution without a clear intention by the patentee to limit the scope of the claims.

31. I understand that extrinsic evidence, such as expert testimony, treatises, or technical dictionaries, may also be relevant to claim construction. However, it is also my understanding that extrinsic evidence is less significant than the intrinsic record of the patent and may not be used to contradict claim definitions that are unambiguous in light of the intrinsic record.

C. Indefiniteness

32. It is my understanding that a patent claim must point out and distinctly claim the subject matter of the invention. I have been informed that a claim is definite when viewed in light of the specification and prosecution history if it informs those skilled in the art about the scope of the invention with reasonable certainty. I understand that the definiteness of a patent claim is evaluated from the perspective of a person of ordinary skill in the art.

33. I also understand that indefiniteness must be proven by clear and convincing evidence to overcome the presumption that an issued patent is valid.

VII. CLAIM CONSTRUCTION

A. The '097 Patent

Term or Phrase	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"ultra-thin resist layer"	No construction is necessary.	Indefinite

34. I have reviewed the Spanos Declaration that I understand was filed in the WDTX litigation.

35. In particular, I have reviewed Dr. Spanos' discussion of the qualifications for a person of ordinary skill in the art (a "POSITA") at the time of the invention with respect to the subject matter of the '097 patent. While I could quibble with certain aspects of that discussion and his definition, his definition is adequate for purposes of interpreting the single term at issue with respect to the '097 patent and I have applied that standard when considering how a POSITA would view the claims of the '097 patent.

36. I am generally familiar with the rules regarding claim construction and patent claims, and I understand that a patent may include independent claims and dependent claims where an independent claim stands alone and includes only the limitations that it recites while a dependent

claim depends from an independent claim or another dependent claim and, as such, includes all of the limitations that it recites in addition to all of the limitations recited in the claim or claims from which it depends.

37. I am informed that the ordinary meaning of a claim term in a patent should be viewed in the context of the written description set out in the specification and also through a review of the prosecution history. Normally, claim terms should be given their ordinary and customary meaning within the context of the patent in which the terms are used, i.e., the meaning that the term would have to a POSITA at the time of the invention in light of what the patent teaches.

38. I understand that a POSITA is deemed to read a claim term not only in the context of the particular claim in which the term appears, but in the context of the entire patent, including the specification. Thus, the words of the claim must be interpreted in view of the entire specification. The specification is the primary basis for construing the claims. Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and what they intended to include within the claim as set forth in the patent itself.

39. I also understand that, if the intrinsic evidence is sufficient to discern the meaning and scope of a particular claim term, it is unnecessary, and indeed improper, to consider extrinsic evidence. I understand that extrinsic evidence may not be used to contradict claim meaning that is unambiguous in light of the intrinsic evidence.

40. I understand that the claims are required to be definite and that definiteness requires that a patent's claims, viewed in light of the specification and file history from the perspective of a POSITA inform those skilled in the art about the scope of the invention with reasonable certainty.

41. I understand that patents and patent claims are presumed valid and that indefiniteness

is an invalidity defense that must be shown by clear and convincing evidence, which is a higher legal standard than a preponderance of the evidence.

42. I am further informed that the doctrine of claim differentiation is merely a rule of thumb that raises a "presumption" that a dependent claim is narrower than the independent claim from which it depends, and that claim differentiation is not a hard and fast rule of claim construction and cannot broaden claims beyond their correct scope. I am further informed that a patent's written description (and its prosecution history) can overcome any presumption that may arise from the doctrine of claim differentiation.

43. I have been asked to opine as to what a POSITA at the time of the invention would have understood by the claim term "ultra-thin resist layer[s]" and whether a POSITA would have understood, based on the claims, specification, prosecution history, and extrinsic evidence, that "ultra-thin resist layer[s]" as used in the patent claims has a defined upper limit and if so, what that upper limit is. In this declaration, I use UTR to refer to "ultra-thin resist" and UTR layer to refer to "ultra-thin resist layer."

44. Based on my review of the '097 patent, whenever the specification discusses an "ultra thin resist layer" (or "UTR layer"), it consistently refers to the layer as having a thickness that is less than 2500 Å.

45. First, when discussing the problems of the prior art, the specification describes that "[a]s the wavelength of the radiation decreases, such classic image exposure techniques cannot be used to satisfactorily generate the pattern line widths ***in the photoresist of less than 0.25 µm (2500 Å)***."[1] ('097 patent at 1:29-32.) The specification then goes on to state that UTR coatings have been developed to overcome this drawback. (*Id.* at 1:34-38.) Then, after describing how the current state-of-the-art involves resist coatings of 5,000 Å for 248 nm lithography and 4,000

[1] Unless otherwise noted, all emphasis in this Declaration has been added.

Å for 193 nm lithography, the specification explicitly sets out a definition of what constitutes an ultra thin resist: "a resist coating having an UTR thickness ***is considered to be*** resist films of less than 0.25 μm (2500 Å) in thickness." (*Id.* at 1:38-45.)

46. While this particular specification discussion refers to a "resist coating," a POSITA would recognize that, as used in the '097 patent, a "resist coating" is substantively the same as a "resist layer" at least when discussing thicknesses.

47. This language establishes the limit or boundary of what qualifies as a thickness of an "ultra thin resist" within the context of the '097 patent.

48. The Description of the Preferred Embodiment section of the '097 patent's specification is wholly consistent. Here are several examples:

- "the problem associated when the conventional lithographic process is applied to an ultra-thin resist thickness of less than 2500 Å will also be explained in connection with FIGS. 2(a) through 2(d)" (*id.* at 2:58-61);
- "when the lithographic process described above in FIGS. 1(a)-1(d) is applied to an UTR thickness of less than 2500 Å, there is created a significant problem. . ." (*id.* at 3:33-37);
- "As can be seen in FIG. 2(a), an UTR layer 18a has a thickness of less than 2500 Å. . ." (*id.* at 3:28-40); and
- "The UTR layer 120 has a thickness of less than 2500 Å" (*id.* at 4:12-13).

Notably, at no point does the '097 patent specification describe an ultra thin layer resist as being any thicker than 2500 Å.

49. I have reviewed the patent's prosecution history but found that it did not contain any particular discussion about "ultra thin resist layers" beyond what is contained in the specification and claims.

50. As a result of these multiple, consistent references to a "thickness of less than2500 Å," a POSITA would have had no difficulty in understanding the meaning of the claim term "ultra thin resist layer" and what the upper thickness boundary of such a layer was intended to be within the context of the invention claimed in the '097 patent.

51. To be sure, claim 4 does explicitly discuss the 2500 Å thickness of the "ultra thin resist layer," making it clear as to the definiteness of this term.

52. A POSITA would readily understand from the '097 patent's specification that the term "ultra thin resist" was used to mean a resist that was less than 2500 Å thick and that an "ultra thin resist layer" for purposes of the '097 patent claims is a resist layer that is less than 2500 Å thick. There is nothing ambiguous about this aspect of the specification's discussion.

53. Consequently, given the clear discussion in the '097 patent specification, it is my understanding that there is no need to examine any extrinsic evidence, such as the multiple unrelated patents discussed by Dr. Spanos at paragraphs 55-58 of his Declaration and in the Defendants' brief at 9-10. Whether or not those patents contain their own specific definitions of "ultra thin resist layers" has no significant bearing on how a POSITA would interpret that term upon reading the specification of the '097 patent.

54. At best, that extrinsic evidence merely indicates that there was some variation as to what was considered to be ultra-thin—and that many of the instances in those patents are wholly consistent with the how the '097 Patent set the boundary for the "ultra thin resist layers" of the claimed invention at 2500 Å—thereby emphasizing the importance of looking to the '097 patent's specification to determine what upper boundary was to be used within the context of the claimed invention.

B. The '651 Patent

Term or Phrase	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"pneumatic cylinder"	No construction is necessary, In the alternative, "a pneumatic, hydraulic, electromagnetic or mechanical device"	"Plain and ordinary" to mean "a cylindrical device that uses pressurized air or other gas to move a shaft of the device in a straight line"

55. I do not believe that the term "pneumatic cylinder" requires construction because the intrinsic record is clear as to its plain and ordinary meaning. To the extent that a construction is required, I agree with Plaintiff's alternative construction, which is "a pneumatic, hydraulic, electromagnetic, or mechanical device."

56. I understand that Defendants disagree with Plaintiffs' alternate construction. According to Defendants, the four mechanisms (pneumatic, hydraulic, electromagnetic, and mechanical) are distinct. I also understand that Defendants have construed this term as "plain and ordinary" which, according to Defendants, means "a cylindrical device that uses pressurized air or other gas to move a shaft of the device in a straight line." For the following reasons, I disagree with Defendants.

57. Addressing Defendants' distinction of the four mechanisms, the specification is instructive. There, the inventor states that "a mechanism useful in adjusting the position of the wafer stage 40 may be comprised of any of variety of devices, such as pneumatic, hydraulic, electromagnetic, or mechanical systems." ('651 patent, 5:65-6:1.) This language suggests that the mechanism that can be used by pneumatic cylinders for adjusting the wafer stage is not limited to only pneumatic; instead, other mechanisms such as hydraulic, electromagnetic, mechanical, or a combination thereof, are similarly contemplated.

58. To be sure, I reviewed but did not find anywhere in the specification that the pneumatic cylinders are limited to the use of only pneumatic mechanism. The specification also does not state anywhere that a "hybrid" cylinder was not contemplated. The use of "or" in the phrase "any of variety of devices, such as pneumatic, hydraulic, electromagnetic, ***or*** mechanical systems," which is disjunctive, also suggests that the inventor did not intend to limit "pneumatic cylinders" to a single mechanism or any particular one.

59. Additionally, a pneumatic cylinder, by definition, is a mechanical device used to generate a force. Inside the pneumatic cylinder is a cavity that utilizes different substance or element for generating that force. In one example, the cavity can be filled with, for example, air or gas to drive a piston in a particular direction in order to generate the desired force. When air or gas is no longer supplied, the piston is returned to its initial position. In this example, the return stroke can be accomplished through the use of, for example, a spring, which is a mechanical component just like the piston. In this example, both pneumatic and mechanical mechanisms are used by the pneumatic cylinders. This type of pneumatic cylidners that utilize both pneumatic and mechanical mechanisms were prevalent during the relevant timeframe.

60. I understand that Dr. Spanos opines that the term "mechanical" refers to "a rack and pinion configuration" where a mechanical device creates the force or motion through interacting with these rack-and-pinion parts. In limiting "mechanical" to only "a rack and pinion configuration," Dr. Spanos appears to opine that pneumatic cylinders are not "mechanical" or adopt mechanical mechanism.

61. I disagree because mechanical mechanism necessarily includes mechanical components, including those described in the specification and shown in Fig. 2 of the drawings. For example, the specification describes the pneumatic cylinder 46 as having mechanical hardware such as a shaft 49, a ball 51 (as part of the ball and socket connection 48), and a valve

61, all of which are and have been used in pneumatic, hydraulic, electromagnetic, and mechanical applications in the relevant timeframe. ('651 patent, 6:21-25.)

62. Additionally, pneumatic cylinders and rack and pinion components are not necessarily exclusive to the other—pneumatic cylinders can include rack and pinion components to form pneumatic rack and pinion actuators such as pneumatic rotary actuators that were commercially available at the time of the invention.

63. I understand that Defendants have made references to the "Pneumatic Systems" book ("PS Book") in support of their construction. That book recognizes "pneumatic cylinders" as "mechanical elements" that include, for example, "piston 9," "piston rod 11," "tie rods 3," and "nuts 6" as shown in Fig. 5.1(b), but does not otherwise disclose any rack and pinion components. Accordingly, there is no basis to interpret mechanical parts as being limited to only rack and pinion components.

64. Pneumatic cylinders also can employ hydraulic mechanism to generate the force needed to move the wafer stage. For example, pneumatic/hydraulic hybrid actuators, which were already in use during the relevant time frame, are one such option.

65. Similarly, in connection with the electromagnetic mechanism, the specification describes the use of electrodes and coils in conjunction with the adjustment of the wafer stage. For example, the inventor explained that "the wafer stage is actually an electrode that is used to ground the wafer while a plasma is created above the wafer by other electrodes or coils in such tools. ('651 patent, 5:19-22.) The inventor also explained that the "adjustable wafer stage 40 . . . may be used to vary the distance between the target (upper electrode) and wafer stage (bottom electrode) in such systems, thereby affecting the deposition rates of the material formed on a wafer . . . ."). (*Id.* at 8:34-39.) In other words, the inventor contemplated that pneumatic

cylinders that employ electromagnetic mechanism (e.g., through electrodes and coils) for adjusting the surface of the wafer stage.

66. The use of electromagnetic mechanism in pneumatic cylinders is also well known at the time of the invention. As discussed above, the use of electrodes and coils can be one means to deploy electromagnetism. Another way to achieve electromagnetic properties is through the cylinders' valves. This is consistent with the specification, which describes these valves as being "used in actuating the pneumatic cylinder 46 to control the position of the surface 42 of the wafer stage 40" ('651 patent, 6:7-11), as is well known to those skilled in the art.

67. The use of such valves to achieve electromagnetic properties in pneumatic cylinders is well known in the field of pneumatics. For example, they have been used in the context of vehicle clutch and transmission (as described in US Pub. No. 2001/0034287 and USP No. 6,524,221), sheet product production (as described in USP NO. 4,111,084), artilleries (e.g., USP No. 4,754,688), and manifolds in piping (e.g., USP No. 5,458,379) at the time of the invention.

68. I understand that Defendants have defined a pneumatic cylinder to be a cylindrical device. But pneumatic cylinders can be, but need not be, cylindrical. For example, many pneumatic cylinders were available in rectangular form at the time of the invention.

69. I understand that Defendants' construction also requires the movement of a shaft in a straight line. I first note that the specification describes a shaft in some embodiments but otherwise does not require the "shaft" to be a component of pneumatic cylinders.

70. Also, I note that both the claims and the specification describe the pneumatic cylinders as being "operatively coupled to said wafer stage to accomplish at least one of raising, lowering, and varying a tilt of said surface of said stage." (*See, e.g.*, claims 1 and 19; *see also* 6:66-7:1.) While moving a shaft, for example, in a straight line, facilitates the raising or

lowering of the wafer stage, doing so does not mean that the shaft could facilitate tilting or varying the angle of the surface of the wafer stage such that the surface could be tilted at an angle. To facilitate tilting, such a shaft would have to be driven off its center of axis. A POSITA would not know how driving the shaft in a straight line, without more, could achieve tilting or varying the tilt angle.

Term or Phrase	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
"said process chamber"	Not indefinite	Indefinite

71. In addition to the term "pneumatic cylinders," I understand that Defendants also have construed the term "said process chamber" recited in claim 31 as indefinite. For the following reasons, I disagree.

72. In claim 31, the first limitation reads: "performing a process operation in a process tool on each of a plurality of wafers." In the next limitation, claim 31 recites "across-wafer variations" resulting from "said process operation performed in said process tool." After measuring across-wafer variations and adjusting the surface of the adjustable wafer stage using the across-wafer variations (third claim limitation), claim 31 then recites "performing said process operation on at least one subsequently processed wafer on said wafer stage in said process chamber" (fourth claim limitation) after the wafer stage has been adjusted.

73. Based on the above, I note that the location of the process operation being performed on the wafers between the first limitation and the fourth limitation is never moved, changed, or modified. In other words, the process operation remains to be performed throughout the method in the process tool that is recited in the first claim limitation.

74. Now, when I read the fourth and last claim limitation, it reiterates that the "said process operation" is being performed on subsequently processed wafers. In other words, it

refers to that same process tool recited in the first claim limitation. As such, the term "said process operation" refers to "the process tool" that is recited in the first and second claim limitations because claim 31 does not recite performing the process operation anywhere else except in the process tool. As a result, I find that it is reasonable certain that the "said process chamber" in the last limitation refers to the "process tool" in the first limitation.

75. My opinion is also confirmed when the dependent claims are examined. For example, there are no dependent claims that recite a process chamber or performing the process operation in places other than the process tool. In the absence of a "process chamber" or any recitation that the process operation is performed elsewhere, it is reasonable certain to one skilled in the art that "said process chamber" in claim 31 means "said process tool."

C. The '538 Patent

76. I have read Dr. Spanos' opinion that the claim term "a significant fault" as used in the '538 patent is indefinite because "[a] POSITA would not be able to understand the scope of this limitation with reasonable certainty." (Spanos Dec. 3 at ¶ 27.) Dr. Spanos' opinion, however, ignores the disclosures of the '538 patent.

77. First, the specification defines "significant faults" when discussing the state of the prior art. For example, the patent discusses how one problem with the prior art to the '538 patent was that fault detection sensors in an IC manufacturing process could not adequately distinguish a fault that resulted in a negative impact to the material being processed, and therefore reported ***any*** deviation from the manufacturing specifications as a fault. ('538 patent at 2:65-67.) According to the patent, in cases where the fault was "small enough that no significant impact to the process was present," the fault report would effectively be a "false positive." (*Id.* at 3:1-3.) The false positive nonetheless triggered an alteration to the manufacturing process. In other

words, the false positive was triggered by a fault that had ***no impact on the material being processed*** "introduce[d] inefficiencies and idle times in a manufacturing setting." (*Id.* at 3:3-4.)

78. The '538 patent specification provides a detailed case of exactly how this inefficient prior art process works. For example, suppose an IC manufacturer recipe maintains small constraints in a pressure sensor at one step of the IC manufacturing process. (*Id.* at 2:60-62.) While manufacturers tried to make the manufacturing process as efficient as possible, a certain amount of "guess work" was required for manufacturers to determine which variances were "significant" and which variances were "harmless." (*Id.* at 3:5-20.) Any variation from the small constraints established by the manufacturer triggered a fault. (*Id.* at 2:62-64.) This was true even if the product of the manufacturing process, an integrated circuit, was not negatively impacted by the pressure variation fault during that manufacturing step (i.e., the pressure sensor fault was "harmless"). (*Id.* at 2:64-67, 3:14-16.) The prior art could not account for the fact that the end product was not impacted by the larger pressure variation, and therefore "introduces inefficiencies and idle times in a manufacturing setting." (*Id.* at 3:3-4.)

79. The '538 patent, however, ***considered this fact that the product being manufactured is not impacted by the insignificant (i.e., not important) fault***. (*Id.* at 5:51-59.) By identifying that the product being manufactured is not negatively impacted by the insignificant fault, the method disclosed in the '538 patent decreases the weight accorded to that type of fault. (*Id.* at 5:51-56.)

80. By decreasing the weight of the insignificant fault in the fault detection analysis, the '538 patent inventions promote efficiency and eliminate at least one type of ultimately unnecessary alteration to the manufacturing process. This is a substantial advantage over the prior art, which required a certain amount of "guess work" to determine the faults that negatively

impact the material being processed (i.e., is "significant") versus the faults that are harmless. (*Id.* t at 2:64-67, 3:14-16.)

81. In my view, the inventors of the '538 patent understood that a POSITA would inherently know that some faults do not impact the end result of the semiconductor manufacturing process, and proceeded based on that understanding.

Term or Phrase	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
"significant fault"	No construction is necessary, or in the alternative, "abnormality or fault that relates to an actual fault".	Indefinite

82. I disagree with Defendants and Dr. Spanos that the term "significant fault" is indefinite within the context of the '538 patent. A POSITA at the time of the invention of the '538 patent, when reading the '538 patent, would not find the claim term "significant fault" to be ambiguous or indefinite, and would have no particular difficulty in understanding the meaning of the term.

83. I believe that their contention ignores the information disclosed in the '538 patent that I discussed above, particularly when they assert that "a POSITA would not have any idea how far a fault must deviate from expected values/faults to be 'significant,' or how out of specification a workpiece must be before experiencing a 'significant' fault. (Defs.' Br. at 31, citing Spanos Dec. at ¶¶ 27, 30.) As I discussed above, the method of the '538 patent considers whether or not the product being manufactured is negatively impacted by a certain fault. ('538 patent at 5:51-59.) If the product is not negatively impacted, the fault is not significant. (*Id.*)

84. Such an understanding is wholly consistent with how a POSITA, or anyone else for that matter, would typically construe "significant," i.e., as something that matters rather than something that has no effect that is worth considering.

Term or Phrase	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"determining in said computer whether said parameter is a significant factor"	No construction is necessary, or in the alternative, "a parameter that provides a significant contribution to the fault"	Indefinite

85. I see that the Defendants and Dr. Spanos largely repeat the same arguments with respect to the use of "significant" in claim 7 when describing whether or not a "parameter" is a "significant factor." I also understand that, if the Court should decide that it needs to construe this term, Ocean proposes that the term be defined as "a parameter that provides a significant contribution to the fault."

86. For much the same reasons as discussed above with respect to the claim term "significant fault," I disagree with Defendants' contention that "a POSITA would not have any idea what the parameter provides to the fault for it to be a 'significant contribution' in the fault." (Defs.' Br. at 33; Spanos Dec. at ¶ 34.)

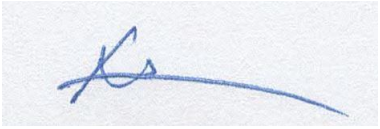
87. In particular, the '538 patent considers whether a product undergoing the manufacturing process is negatively impacted by a parameter (i.e., the factor is significant) or not (i.e., the factor is harmless). ('538 patent at 5:51-59.) In other words, the '538 patent's specification supports Ocean's proposed construction: the computer determines whether the parameter "provides a significant contribution to the fault." (*Id.* at 5:51-56.)

88. A POSITA at the time of the invention of the '538 patent, when reading the '538 patent, would not find the claim term "determining in said computer whether said parameter is a

significant fault" to be ambiguous or indefinite, and would have no particular difficulty in understanding the meaning of the term.

89. I hereby declare that all statements made herein of my own knowledge are true and that all statements are made on information and are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001.

Dated: October 25, 2021



Ron Maltiel

EXHIBIT 1

RON MALTIEL

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PROFESSIONAL SUMMARY:

Mr. Maltiel is a senior member of IEEE with more than 30 years experience in all phases of design and implementation of computer semiconductor devices. He has worked in the development and production of storage technology and semiconductor devices such as Dynamic Ram (DRAM), Flash (NAND, NOR), SSD, EEPROM, ROM, and Static RAM (SRAM) memories which were used in microprocessors, logic, digital, and analog products.

Mr. Maltiel studied semiconductors at Stanford University graduate school and went on to work at Intel, AMI, AMD, and Maxim. His teams included circuit, process, and device engineers and was responsible for integrating all of the various disciplines into one working product. Mr. Maltiel holds six semiconductor device, process, and measurement patents which have been cited more than 130 times.

Currently, Mr. Maltiel is an independent consultant in the areas of semiconductor design, process and manufacturing and has been retained as an expert witness on many patent cases. In addition, Mr. Maltiel maintains an informational website and database which is regularly visited by USPTO, US Department of Justice, technology departments, attorneys, and investors from 99 countries. He is also fluent in Hebrew.

EXPERTISE:

Circuit and Process Development:
- Analog
- DRAM
- Flash / EEPROM and ROM
- SRAM
- pMOS, nMOS, and CMOS
- High voltage BICMOS

Process Steps Development:
- Process flow design
- Gate and polysilicon oxidation steps
- Metal deposition and barrier layers steps
- Etching, laser definition, poly or metal deposition and planarization process steps such as Chemical Mechanical Polishing (CMP)
- Plasma and Trench etching steps
- Cleaning and wafer gettering methods

Devices Development:
- DRAM memory cells
- SRAM memory cells
- Flash / EEPROM and ROM memory cells
- Precision resistors and capacitors
- Transistors/ resistors/capacitors/JFET in FinFET, pMOS, nMOS, CMOS, and BICMOS processes
- Polysilicon - polysilicon capacitors
- PNP and NPN transistors

Test Chip Development:
- Created a library of test chip structures for process, ESD circuits, design rules, and device evaluation using GDS tools.
- Measured test structures and evaluated their device properties

R O N M A L T I E L

PROFESSIONAL EXPERIENCE

INDEPENDANT CONSULTANT, 1993 - present

- Provides consulting in various aspects of semiconductor technology and semiconductor manufacturing.
- Provides expert technical consultations and has testified at trials.
- Designs and operates a popular semiconductor technology web site which includes current developments in the digital and analog fields such as DRAM, Flash (NAND, NOR), SSD, EEPROM, ROM, and SRAM. The site includes tutorials and educational information, industry news and resources, acronym and technical word definitions, and patent search or patent application information, and is regularly visited by major technology companies and universities from 99 countries.

MAXIM INTEGRATED PRODUCTS , 1989 - 1993

- Personally developed a high voltage BICMOS device, introduced it to production, and proved the feasibility of adding an EEPROM element to it.
- Established MAXIM processes in a newly purchased fab, developed the company's newest analog process, installed MAXIM's production in a new foundry, and managed the relationship.

ADVANCED MICRO DEVICES , 1983 -1989

- Managed consolidation of test chip development through the building of a company-wide standard test chip library. As a direct result of this project, the time needed to build test chips was reduced by 60%, structures were improved, and test program generation was accelerated.
- Contributed to development of 256k SRAM, including process flow, a backend planarization scheme, and overseeing the building of generic test chip library.
- Participated in defining 1M CMOS DRAM memory and proved feasibility of integrating trenches in the process. Coordinated the development of post groove planarization process and double poly module. The project ended successfully with a working first silicon.
- Developed and proved feasibility of integrating EEPROM with DRAM CMOS process and devices. Reduced cell size by 40%, process steps by 15%, and improved EEPROM programming operation.

AMERICAN MICROSYSTEMS, INC., 1982 - 1983

- Introduced and established the EEPROM device. Directed the design of the test chip, process flow determination, manufacture of several working runs and measurement of the electrical parameters.
- Created a new process approach that improves poly dielectric strength and founded a new cell structure with multiple benefits over existing cells.

INTEL , 1980 - 1982

Participated in the development of EEPROM technology with particular emphasis on the reliability aspects such as charge retention and cycling endurance. Work involved the study of failure mechanisms, making the necessary process changes, and evaluating the results. Regular interaction with fab and technology development was required. Improved operator utilization by 20%.

STANFORD UNIVERSITY , 1978 - 1980

- E.E. research group on metallic impurities and their electrical behaviors.
- Independent research included manufacturing of Si devices and electrical measurements of their properties.

EDUCATION

Engineer Degree, Material Science Engineering, Stanford University, 1980
MS, Material Science and Engineering, Stanford University, 1978
BS, Material Science and Engineering, Ben-Gurion University, 1977

PATENTS

Mr. Maltiel's patents have been cited more than 130 times

- Electrical measurements of profile of semiconductor devices during their manufacturing process - #4,978,923
- Method and apparatus for non-destructive data in a shadow memory array - #4,716,552
- Electrical measurements of properties of semiconductor devices during their manufacturing process - # 4,956,611
- Memory cell providing simultaneous non-destructive access to volatile and non-volatile data - #4,672,580
- Non-volatile dynamic ram cell - #4,611,309
- Gold-doped IC resistor region - #4,432,008

PROFESSIONAL AFFILIATIONS

IEEE Senior Member
IEEE Device Society
IEEE Circuits Society
IEEE Communications Society
IEEE-USA Consultants Database
Jewish High Tech

LITIGATION RELATED EXPERIENCE

Expert Engagements

Type of Matter:	Patent Infringement
Law Firm:	Devlin Law Firm
Case Name:	**Ocean Semiconductor** vs Analog Devices, Infineon, and Renesas.
Services Provided:	Technical consulting expert on semiconductor development and manufacturing case. Reviewed infringing patents. Wrote declarations.
Date:	2020-1

Type of Matter:	Patent Infringement
Law Firm:	Quinn Emanuel
Case Name:	**IP Bridge** vs Micron.
Services Provided:	Technical consulting expert on semiconductor development and manufacturing case. Reviewed infringing patents, contact and metallization manufacturing processes, and layout files. Wrote a declaration and the case was settled successfully.
Date:	2020

Type of Matter:	Patent Infringement
Law Firm:	Mintz Levin
Case Name:	**Innovative Foundry Technologies** Inc. vs TSMC.
Services Provided:	Technical consulting expert on semiconductor development and manufacturing case. Reviewed infringing patents, defendant's FinFET, contact and metallization manufacturing processes, and GDS layout files. Assisted in overseas depositions where the case was settled successfully following the depositions.
Date:	2018-9

Type of Matter:	Patent Infringement
Law Firm:	Nixon Peabody LLP
Case Name:	Lone Star Silicon Innovations Inc. vs **Nanya Technology**.
Services Provided:	Testifying expert and technical consultant on semiconductor development and manufacturing in IPR cases. Wrote the expert reports and was deposed.
Date:	2017-8

Type of Matter:	Patent Infringement
Law Firm:	TechKnowledge Law Group LLP
Case Name:	**ProMos** vs Samsung.
Services Provided:	Testifying expert and technical consultant on semiconductor development and manufacturing in IPR cases. Wrote the expert reports and was deposed.
Date:	2017-8

Type of Matter:	Patent Infringement
Law Firm:	Sidley Austin
Case Name:	Netlist vs **Hynix**.
Services Provided:	Testifying expert and technical consultant on semiconductor product and device operations in an IPR Cases. Wrote the expert reports and was deposed.

Date:	2016-7
Type of Matter:	Patent Infringement
Law Firm:	Fitzpatrick, Cella, Harper & Scinto
Case Name:	Intellectual Ventures vs. **Canon**.
Services Provided:	Testifying expert and technical consultant on semiconductor product and photovoltaic device operations. Case was settled following my deposition.
Date:	2015
Type of Matter:	Patent Infringement
Law Firm:	TechKnowledge Law Group LLP
Case Name:	**Home Semiconductor** vs. Samsung.
Services Provided:	Testifying expert and technical consultant on semiconductor device operations.
Date:	2014 – 15
Type of Matter:	Patent Infringement
Law Firm:	Vinson & Elkins LLP
Case Name:	Round Rock Research vs. **Sandisk Corp.**
Services Provided:	Testifying expert and technical consultant on patents relating to the manufacturing and operation of semiconductor memory in a system. Wrote invalidity and exhaustion declarations, was deposed, prior art searches, and analyzed patent infringements and validity. Several of the patents were dropped from the case following my declarations. Plaintiff withdrew case prior to trial.
Date:	2013 – 14
Type of Matter:	Patent Board Declaration
Law Firm:	Oblon, Spivak, McClelland, Maier & Neustadt, L.L.P
Case Name:	NXP B.V. vs. **Research In Motion**
Services Provided:	Prepared declarations for the Patent Board Patent Trial and Appeal Board of the US Patent and Trademark Office regarding semiconductor development and manufacturing.
Date:	2013 - 14
Type of Matter:	Patent Infringement
Law Firm:	Undisclosed
Case Name:	Undisclosed
Services Provided:	Technical consultant regarding semiconductor development and manufacturing. Prior art searches, analyze patents infringement and validity.
Date:	2012 – 13
Type of Matter:	Patent Infringement
Law Firm:	Agility IP Law, LLP
Case Name:	**Keranos** vs. Analog Devices
Services Provided:	Technical consultant regarding semiconductor non volatile memory devices, wrote declarations, was deposed, and analyzed patents infringement and validity.
Date:	2012 – 13
Type of Matter:	Patent Infringement
Law Firm:	Undisclosed
Case Name:	Undisclosed

Services Provided:	Technical consultant regarding semiconductor Flash and DRAM memory circuits, prior art searches, analyze patents infringement and validity.
Date:	2012

Type of Matter:	Patent Infringement
Law Firm:	Barnes & Thornburg LLP
Case Name:	**Creative Integrated Systems** vs. Nintendo
Services Provided:	Testifying expert and technical consultant for the operation of semiconductor memory in a system. Wrote declarations, was deposed and testified in court.
Date:	2010 - 13

Type of Matter:	Patent Infringement
Law Firm:	Duane Morris LLP
Case Name:	**e.Digital** vs. Pentax
Services Provided:	Testifying expert and technical consultant for the operation and storage of Flash memory in a system. Analyzed the product and prior art searches, reviewed patent file wrapper, and was deposed. Patent reexamination evaluation.
Date:	2009 - 11

Type of Matter:	Antitrust
Law Firm:	Susman Godfrey LLP
Case Name:	**Tessera Technologies** vs. Hynix Semiconductors case no. 1-06-cv-076688
Services Provided:	Testifying expert and technical consultant for the operation of DRAM memory system. Analyzed company's methodologies of bringing new technology to the market and prior art searches, reviewed depositions, was deposed;
Date:	2009 - 11

Type of Matter:	Patent Infringement
Law Firm:	Undisclosed
Case Name:	Undisclosed
Services Provided:	Computer system testifying expert, technical consulting, prior art searches, analyze patents infringement and validity.
Date:	2008 - 9

Type of Matter:	Patent Infringement
Law Firm:	Munger, Tolles & Olson LLP
Case Name:	Hynix vs. **Rambus**
Services Provided:	DRAM Memory testifying Expert, technical consulting for Rambus. Was deposed and provided expert report. Witness testimony provided in March 2008. Rambus won the case on all claims. Jury stated they found Mr. Maltiel the more believable expert.
Date:	2007 - 8

Type of Matter:	Patent Infringement
Law Firm:	White & Case LLP
Case Name:	Hynix vs. **Rambus** - European Commission in Brussels, Belgium
Services Provided:	DRAM Memory testifying Expert, technical consulting, provided expert report.
Date:	2007 - 8

Type of Matter: P	Patent Infringement
Law Firm:	Undisclosed
Case Name:	Undisclosed
Services Provided:	Non volatile memory expert consultant, patent infringement analysis, and preparation for expert witness testimony
Date:	2006

Type of Matter:	Wrongful Termination
Law Firm:	Jordan Kushner
Case Name:	Undisclosed
Services Provided:	Evaluate quality of technical work in case where employee was fired. Was deposed and provided expert declarations
Date:	2003

Type of Matter:	Patent Infringement Matters (3)
Law Firm:	Venable Baetjer
Case Name:	**Patent Enforcement Fund** vs. NEC
Services Provided:	Semiconductor memory expert consultant, technical consultant, develop trade secret violation list, prior art searches, analyze patent's infringement and validity. Provided several expert reports and declarations. Deposed for several days
Date:	Approximately 3 separate cases various dates between 1993 and 1995

Consulting Engagements

Type of Matter:	Patent Infringement
Law Firm:	Fish and Richardson
Case Name:	Undisclosed
Services Provided:	Expert consultant and prior art searches of ESD circuits
Date:	2007

Type of Matter:	Patent Infringement
Law Firm:	Townsend and Townsend
Case Name:	Undisclosed
Services Provided:	Expert consultant and prior art searches of EEPROM memory
Date:	2006

Type of Matter:	Patent Infringement
Law Firm:	Undisclosed
Case Name:	Undisclosed
Services Provided:	Non volatile memory device expert consultant, technical consulting, and preparation for Expert Witness testimony
Date: 2006	

Type of Matter:	Theft of Trade secrets, Patent Infringements
Law Firm:	Paul Hasting

R O N M A L T I E L

Case Name:	Undisclosed
Services Provided:	Expert consultant, prior art searches, analyze patents.
Date:	2004

Type of Matter:	Patent Infringement and Theft of Trade Secret Matters
Law Firm:	Heller Ehrman LLP
Case Name:	**Atmel** vs. ISD Services Provided:. EEPROM device and circuits expert consultant, technical consultant, develop trade secret violation list, prior art searches, analyze patent's infringement and validity, EEPROM circuits infringement analysis, mask layers evaluation, ESD structures analysis. For several years worked full time as an outside expert on various EEPROM and other cases.
Date:	Approximately 6 separate cases various dates 1995 to 2000